REMARKS

This Amendment is submitted in response to the Office Action dated June 16, 2004, having a shortened statutory period set to expire September 16, 2004. Claims 1-2, 4, 6, 8, 9-10, and 13-15 have been amended, and claims 1-16 are currently pending.

Objections to the Drawings

A proposed amendment to Figure 1 is included herewith in response to the objection that Figure 1 failed to include the reference signs "1" and "0" between nodes A and C and that it is unclear how RT5 01010 relates to the figure. However, Applicants traverse the contention that the significance and meaning of character strings "10111", "10101" and "10011" is not adequately disclosed in Figure 1 and the corresponding specification text. As depicted in Figure 1, node G selects between two branches in accordance with a five-bit pattern analysis as adequately explained in the specification at page 8, lines 1-7 (selects right hand branch responsive to a "10111", "10101" or "10011" result, else the left hand branch is selected).

Figure 5 and the specification have been amended herein in responsive to the objection that several reference signs that were not clearly demarcated in the description. Specifically, reference numerals have been included into the amended Figure 5 with corresponding referencing in amendments to paragraphs in the specification at page 14, line 28, page 15, line 10, page 15, line 22, page 15, line 29, and page 16, line 6.

Objections to the Specification

The abstract of the disclosure has been amended herein to comply with the 150 word limit and the application title has been moved to that only the abstract paragraph follows the heading "Abstract of the Disclosure".

The specification at page 1, line 11, page 9, lines 15, 19 and 32 and claim 8 have been amended as suggested in the Office Action. Regarding the objection to Fig. 4, however, Applicants have submitted herewith an amended Figure 4 which includes a line for element 40 and in which the Instruction Address (InsAD) has been properly relocated.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-3, 5, and 9-11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,917,824, issued to Gobuyan et al. (hereinafter *Gobuyan*) in view of U.S. Pat. No. 6,026,473, issued to Cross et al. (hereinafter *Cross*). Applicants respectfully traverse the foregoing rejections as they may apply to the pending claims as amended herein for the following reasons.

Regarding the grounds for rejecting independent claims 1 and 9, Applicants agree that *Gobuyan* discloses packet processing including simultaneous processing of source and destination address fields. Applicants disagree, however, that *Cross* teaches a "task scheduler" for enabling a first bank of registers to transfer an instruction loaded therein for processing by a task processor and for enabling a second bank of registers to transfer an instruction loaded therein for processing by the task processor. As explained at col. 2, lines 47-59, Cross discloses a control unit and a write-address counter for alternately enabling even and odd hold registers and to alternately address even and odd latch-based memory banks. *Cross* includes no discussion of transferring instructions to any kind of processor.

Furthermore, Applicants point out that *Gobuyan* discloses a lookup engine that employs a destination address lookup engine 1 that operates in *parallel* with a source address lookup engine 2 (see Figure 3, col. 2, lines 32-36) to achieve simultaneous resolution of the source address (routing) and destination address (filter) data contained in a packet. As explained in Applicants' background at page 3, lines 3-10, Applicants' proposed invention is expressly directed to improving the bifurcated routing/filter processing of packets in which substantial hardware and processing overhead are required for conventional parallel configured systems such as that taught by *Gobuyan*. Neither *Gobuyan* nor *Cross* provide and motivation or suggestion to combine the alternating-cycle register enabling feature taught by *Cross* with *Gobuyan's* parallel processing design. Absent the teachings set forth in Applicants' specification, figures and claims, no motivation or suggestion exists in the art for combining these references in this manner.

The foregoing traversal notwithstanding, independent claims 1 and 9 have been amended to further characterize and distinguish Applicants' proposed invention. Amended claim 1 now recites a system for processing a packet, that in addition to the source and destination centric register banks further includes:

"instruction load means for loading said first and second bank of registers;" and

"a task scheduler that enables said instruction load means to load a next instruction to said first bank of registers and enables said second bank of registers to transfer an instruction loaded therein for processing by said task processor during a first time cycle domain, wherein said task scheduler further enables said instruction load means to load a next instruction to said second bank of registers and enables said first bank of registers to transfer an instruction loaded therein for processing by said task processor during a second time cycle domain that is interleaved in an alternating manner with said first time cycle domain." Independent method claim 9 has been amended to substantially include these same features.

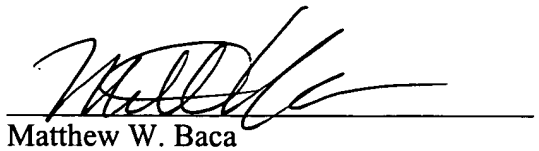
Ample support for the foregoing elements is provided in Applicants' specification, particular with reference to Figures 2, 3 and 4 (depicting instruction load means in the form of address register 44 and memory 12 and task scheduler 18 and associate timing diagram in Figure 3).

Neither *Gobuyan* nor *Cross*, individually or in combination, teach or suggest a packet processing method or mechanism in which simultaneous destination address and source address analysis is conducted by use of an interleaved instruction load/process by which source address instructions are loaded while destination address instructions are processed in one time cycle domain (i.e. an even or odd time cycle) and vice versa for the alternate time cycle domain. It is therefore submitted that independent claims 1 and 9 and all claims depending therefrom have been placed in condition for allowance and a notice to that effect is respectfully requested.

No extension of time is believed to be required. However, in the event that an extension of time is required, please charge that extension fee and any other required fees to **IBM Corporation Deposit Account Number 09-0457.**

Applicants invite the Examiner to contact the undersigned attorney of record at (512) 343-6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



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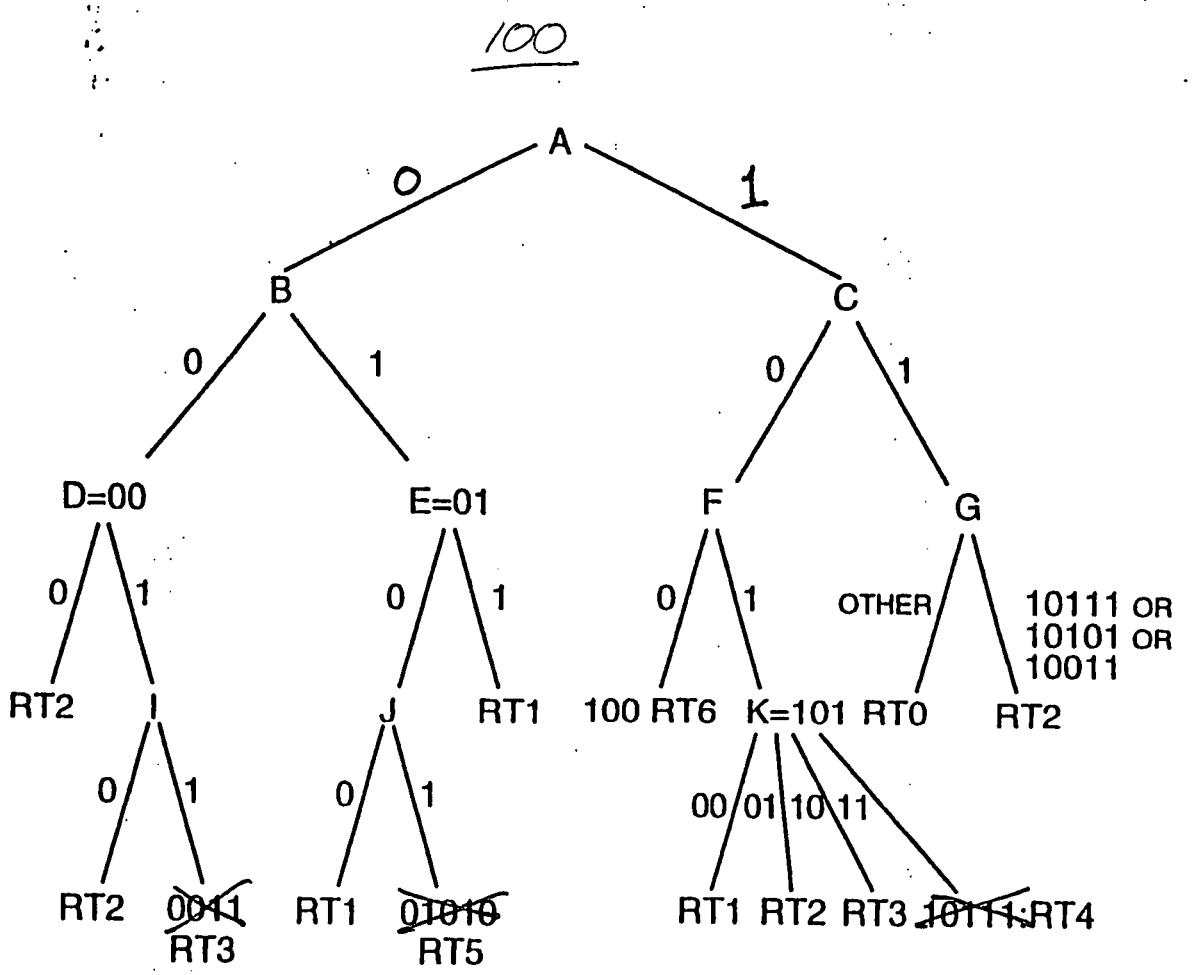

FIG. 1

(Amended)

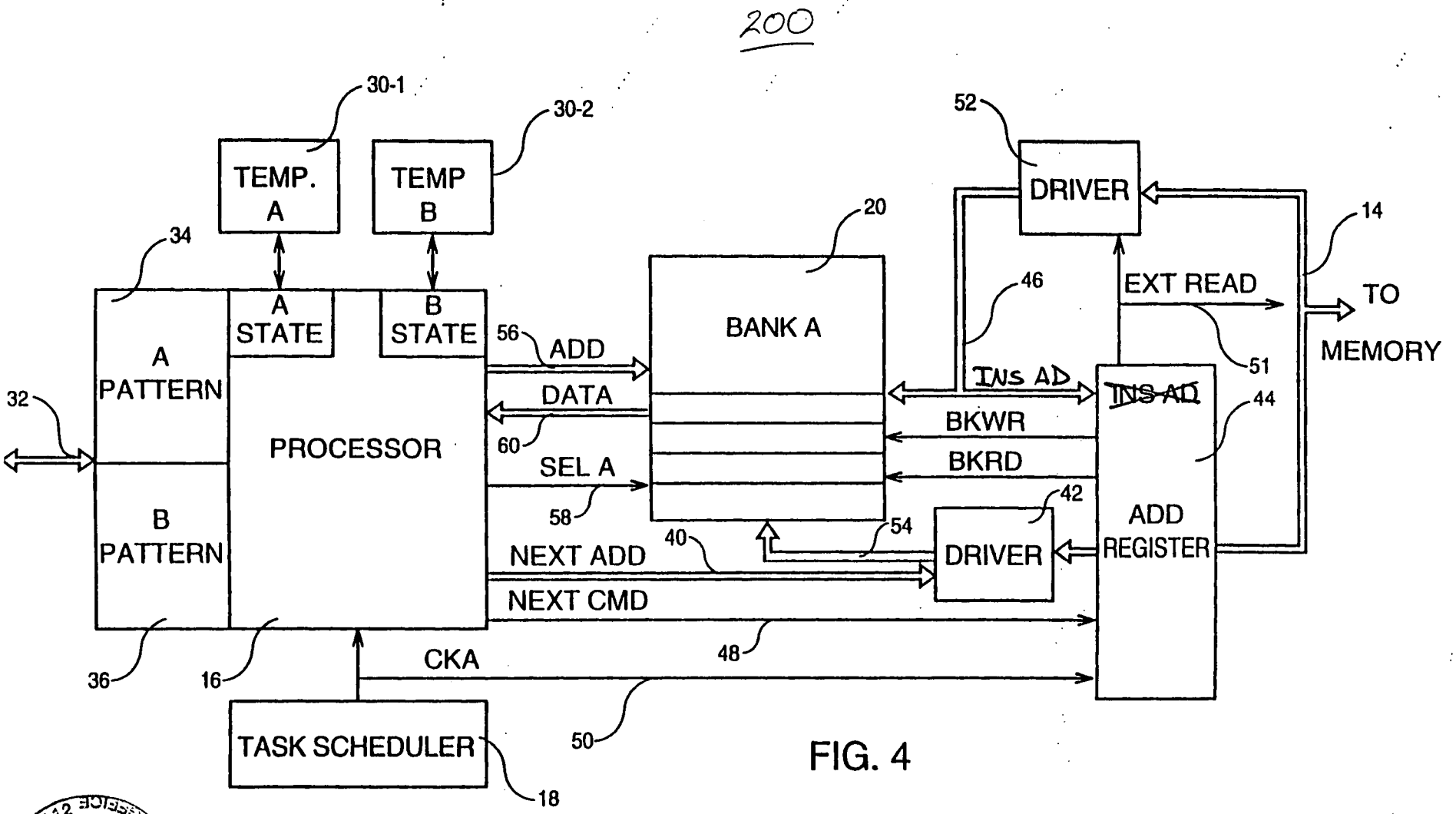

FIG. 4

(Amended)

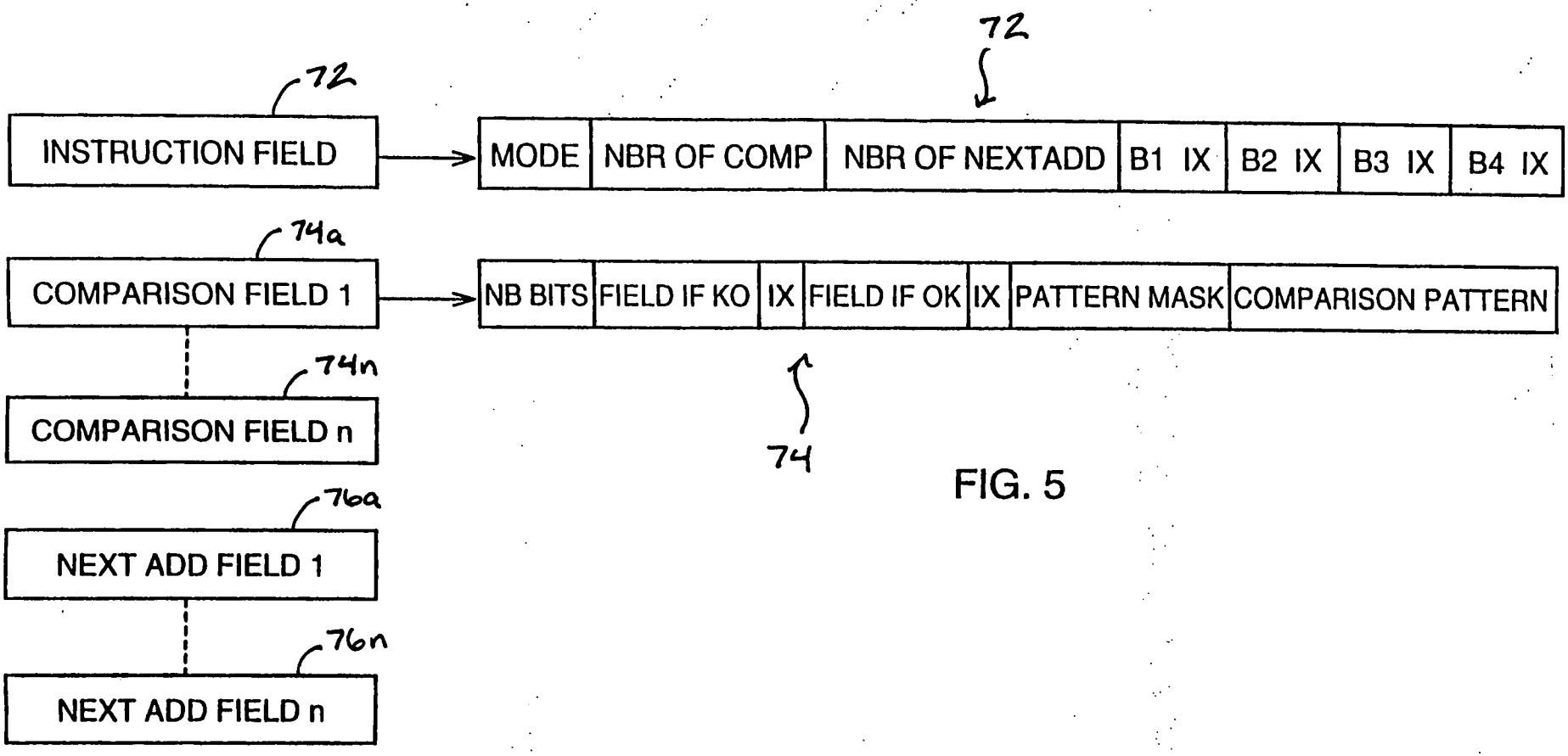

FIG. 5

(Amended)